

REMARKS/ARGUMENTS

The present amendment is submitted in response to the Office Action received from the United States Patent Office dated May 25, 2010. The Patent Office rejected Claims 1-11 under 35 U.S.C. §103(a) as being anticipated by *Hovell et al.* (U.S. Patent Number 7,116,681) in view of *Hies et al.* (U.S. Patent Number 7,333,510).

Applicant respectfully submits that the explanations below overcome the rejections to the claims. Applicant submits that all of the claims are now in condition for allowance. Notice to that effect is requested.

The Patent Office has rejected Claims 1-11 under 35 U.S.C. §103(a) as being anticipated by *Hovell et al.* (U.S. Patent Number 7,116,681) in view of *Hies et al.* (U.S. Patent Number 7,333,510) alleging that Claim 1, *Hovell et al.* discloses a communication protocol converter comprising: (a) a first modular communication jack having: a housing defining an open cavity and a segregated interior chamber, a connector port having a plurality of electrical contacts positioned within said open cavity, at least one circuit board incorporating Ethernet to raw data conversion circuitry components for a first communication protocol disposed within said interior chamber in electrical communication with the electrical contacts of said connector port; wherein the circuitry components are positioned on both sides of the at least one circuit board (ports connecting 62(A, B) and 72(A, B) of fig. 2, see fig. 2, col.8 line 10 to col.9 line 20); and iv) a memory positioned on said circuit board in electrical communication with said conversion circuitry for a first communication protocol for receiving converted data (using network controller to process data conversion, see figs.1, 2, col.6 line 13 to col.7 line 50); whereby the memory is interconnected to a bi-directional data line that allows the input and output of raw data (writing and accessing data from/to the storage (68A fig. 2), see col.8 line 10 to col.9 line 20) (b) a second modular communication jack having: i) a housing defining an open cavity and a segregated interior chamber; ii) a connector port having a plurality of electrical contacts positioned within said open cavity; iii) at least one circuit board incorporating Ethernet to raw data conversion circuitry components for a second communication protocol disposed within said interior chamber in electrical communication with the electrical contacts of said connector port; a

memory positioned on said circuit board in electrical communication with said conversion circuitry for said second communication protocol for receiving converted data (see fig. 2, col.7 line 17 to col.8 line 58) wherein the memory is connected with the bi-directional line to receive input of raw data from the first modular communication jack; and (c) a bidirectional data interface electrically interconnecting said memory of said first communication jack with said memory of said second communication jack (processing data in/out of the storage, see col.8 lines 10-58).

The Office Action admits, however, that *Hovell et al.* does not specifically disclose a controller block in the form of a microprocessor which handles all the conversion between raw data and Ethernet, including processing of digital and analog signals, as well as all of the required code protocol translations, said microprocessor utilizing embedded software to manipulate the data signal to provide data to magnetics and the memory for storing data utilized by a controller block and to communicate with Ethernet through Ethernet interface. However, the Office Action alleges that *Hies et al.* discloses a controller block in the form of a microprocessor which handles all the conversion between raw data and Ethernet, including processing of digital and analog signals, as well as all of the required code protocol translations, said microprocessor utilizing embedded software to manipulate the data signal to provide data to magnetics and the memory for storing data utilized by a controller block (memory block 65 fig. 6) and to communicate with Ethernet through Ethernet interface for storing data that utilized by a controller block (memory block 65 fig. 6) (using a CPU to control routing table computations and performing protocol conversions from IPV4 to IPV6 and a memory block to control the operating system or applications using Ethernet interfaces, see fig. 6, col.6 line 24 to col.7 line 58). The Patent Office states it would have been obvious to one of the ordinary skill in the art at the time the invention was made to implement *Hies et al.* teachings into the *Hovell et al.*'s converter to process data information because it would have allowed the master processor to efficiently perform routing computations, network diagnostics in a communication network (see *Hies*' col.7 lines 2-23).

The Patent Office alleges that as to Claim 7, *Hovell et al.* discloses a communication protocol converter comprising: a housing defining first and second open cavities and a segregated interior chamber; each of said open cavities incorporating a plurality of electrical contacts positioned within said open cavities to form first and second connector ports wherein

said first connector port is adapted to interface with a first communication protocol and said second connector port is adapted to interface with a second communication protocol (using network controller to process data conversion, see figs.1, 2, col.6 line 13 to col.7 line 50); and at least one circuit board incorporating communication protocol conversion circuitry components disposed within said interior chamber in electrical communication with the electrical contacts of said first and second connector ports wherein said conversion circuitry bi-directionally translates communication protocols (network protocol translation, see fig. 2, col.7 line 17 to col.8 line 58), wherein the housing allows for the at least one circuit board to electronically communicate with both the first connector port and the second connector port and a microprocessor employing embedded software that converts Ethernet data from internet protocol version 4 to internet protocol version 6 (converting data from IPV4 to IPV6, see fig. 2, col.7 line 17 to col.8 line 58).

The Patent Office alleges that *Hovell et al.* does not specifically disclose a microprocessor to receive Internet protocol 4 Ethernet data, removes the Internet protocol 4 header data, inserts Internet protocol 6 header data, recalculates the necessary Internet protocol header fields and outputs corresponding Internet protocol 6 Ethernet data and a embedded software located on flash memory which is utilized by the microprocessor to perform its functions. However, the Office Action alleges that *Hies et al.* discloses a microprocessor receive Internet protocol 4 Ethernet data, removes the Internet protocol 4 header data, inserts Internet protocol 6 header data, recalculates the necessary Internet protocol header fields and outputs corresponding Internet protocol 6 Ethernet data and a embedded software located on flash memory which is utilized by the microprocessor to perform its functions (memory block 65 fig. 6) (using a CPU to control routing table computations and performing protocol conversions from IPV4 to IPV6 and a memory block to control the operating system or applications, see fig. 6, col.6 line 24 to col.7 line 58). The Patent Office alleges it would have been obvious to one of the ordinary skill in the art at the time the invention was made to implement *Hies et al.*'s teachings into the *Hovell et al.*'s converter to process data information because it would have allowed the master processor to efficiently perform routing computations, network diagnostics in a communication network (see *Hies et al.*'s col.7 lines 2-23).

With respect to independent Claim 1, the Office Action alleges that *Hies et al.* teaches “a microprocessor which handles all the conversion between raw data and Ethernet, including processing of digital and analog signals” as recited in claim 1. (Office Action, p. 4, emphasis

added.) As illustrated in fig. 6 of *Hies et al.*, processor 63 clearly does not “handle[] all the conversion between raw data and Ethernet, including . . . analog signals” because processor 63 is connected to interface 68 over bus 15. *Hies et al.* fails to provide any further details on how the processor converts data in its specification, any analog signals received at interface 68 would have to be converted to digital signals and then read or written to the processor 63 over bus 15. Applicants note that bus 15 of *Hies et al.* can be a digital bus such as a PCI bus. Even if another type of bus was used, nothing in *Hies et al.* teaches or even suggests that the bus used can connect analog signals to processor 63.

With respect to independent Claim 7, the Office Action alleges that *Hies et al.* “discloses a microprocessor receive Internet protocol 4 Ethernet data, removes the Internet protocol 4 header data, inserts Internet protocol 6 header data, recalculates the necessary Internet protocol header fields and outputs corresponding Internet protocol 6 Ethernet data.” (Office Action, p. 6.) Nothing in *Hies et al.* teaches or suggests the processor “handles all the conversion between raw data and Ethernet, including processing of digital and analog signals” as recited in Claim 7. As discussed above, *Hies et al.*, processor 63 clearly does not process analog signals because processor 63 is connected to interface 68 over bus 15. In other words, the prior art references require additional structural elements or processes in order to perform the communication protocol conversion taught in the present invention.

Additionally, the Office Action alleges that *Hies et al.* teaches “embedded software located on flash memory which is utilized by the microprocessor to perform its function (memory block 65 fig. 6).” (Office Action, p. 6.) Nothing in *Hies et al.*, teaches or suggests that the memory is flash memory.

It is further submitted that the question under §103 is whether the totality of the art would collectively suggest the claimed invention to one of ordinary skill in this art. *In re Simon*, 461 F.2d 1387, 174 USPQ 114 (CCPA 1972).

That elements, even distinguishing elements, are disclosed in the art is alone insufficient. It is common to find elements somewhere in the art. Moreover, most if not all elements perform their ordained and expected functions. The test is whether the invention as a whole, in light of the teaching of the reference, would have been obvious to one of ordinary skill in the art at the

time the invention was made. *Connell v. Sears, Roebuck & Co.*, 722 F.2d 1542, 220 USPQ 193 (Fed. Cir. 1983).

It is insufficient that the art disclosed component's of Applicants' invention. A teaching, suggestion, or incentive must exit to make the combination made by Applicants. *Interconnect Planning Corp. v. Feil*, 774 F.2d 1132, 1143, 227 USPQ 543, 551 (Fed. Cir. 1988).

As set forth in MPEP § 2143(A), “[t]he rationale to support a conclusion that the claim would have been obvious is that all the claimed elements were known in the prior art and one skilled in the art could have combined the elements as claimed by known methods with no change in their respective functions, and the combination yielded nothing more than predictable results to one of ordinary skill in the art.” (underlining added for emphasis). MPEP § 2143(A), p. 2100-129, Eighth Edition, Rev. 6, Sept. 2007. Further, as set forth in MPEP § 2143.01, under *KSR*, “[i]f the proposed modification or combination of prior art would change the principle of operation of the prior art invention being modified, then the teachings of the references are not sufficient to render the claims *prima facie* obvious.” MPEP § 2143.01, p. 2100-141, Eighth Edition, Rev. 6, Sept. 2007.

In view of the foregoing remarks and amendments, the rejection of Claims 1-11 under 35 U.S.C. §103(a) as being anticipated by *Hovell et al.* in view of *Hies et al.* has been overcome and should be withdrawn. Notice to that effect is requested.


Claim 2-6 depend from Claim 1; Claims 8-11 depend from Claim 7. These claims are further believed allowable for the same reasons set forth with respect to independent Claims 1 and 7 since each sets forth additional novel steps of Applicant's Communication Protocol Converter and Method of Protocol Conversion.

In view of the foregoing remarks, Applicant respectfully submits that all of the claims in the application are in allowable form and that the application is now in condition for allowance. any outstanding issues remain, Applicant urges the Patent Office to telephone Applicant's attorney so that the same may be resolved and the application expedited to issue. Applicant requests the Patent Office to indicate all claims as allowable and to pass the application to issue.

Respectfully submitted,
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